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SECTION 1. SYSTEM DESCRIPTION, AFT INTEGRATED ELECTRONICS ASSEMBLY (IEA)

The electrical system is defined by the SRB OF Electrical Schematics (USA SRBE DWG No. 10400-0833). (All Failure Causes)

A. Power Distribution Circuits

(1) To preclude the loss of orbiter power bus C and A or B per listed failure modes, power is provided in electrically isolated redundant systems (channels) to the Aft IEA. The Aft IEA design provides one common housing with a metal wall separating the redundant A and B channels. Power bus C is routed in the same side as power bus A, but separated by its shield from other IEA wiring. The IEA is pressurized with dry nitrogen to assure that fire cannot propagate between power bus C and other IEA circuits. Power bus C is not connected to any equipment in common with power bus A or B. Listed failure modes (except as noted for Bus C) could be caused by specific failures in the Electromagnetic Compatibility (EMC) filters, transorb lightning suppression diodes, Power Bus Isolation Supply (PBIS) modules, solid state switches, APU BITE Card, APU Controller Card or wiring harnesses in the distributor or signal conditioner. (Only distributor wiring harness failures can affect power bus C.)

(2) To preclude the loss of both Aft OF MDMs per listed failure mode, redundant Orbiter A and B buses provide power to the Aft Of MDM housed in the Aft Integrated Electronics Assembly (IEA). The Aft IEA design provides one common housing with a metal wall separating and isolating the redundant A and B channels. This failure mode could be caused by specific failures in the A and B Distributor harnesses. The failure of one Orbiter bus to the Aft OF MDM would result in loss of all MDM outputs for that channel, including the APU start commands.

B. SRM Chamber Pressure Measurement Circuit

To preclude the loss of SRM chamber pressure measurements per listed failure mode, redundant signal paths for sensors A, B and C are provided through the Aft IEA. The B sensor output is routed via twisted, shielded wires through the B channel of the Aft IEA. The A and C sensor outputs are routed via separate twisted, shielded wire pairs through the A channel of the Aft IEA. Each sensor output is routed into and out of the Aft IEA through separate connectors. No two sensor outputs are routed through a common connector or within a common shield.

C. Rate Gyro Output Circuit

To preclude loss of RGA outputs per listed failure mode, separate wiring paths have been provided for each RGA with a metal wall separating the redundant A and B channels. Pitch and yaw outputs from two RGAs are routed through the lefthand Aft IEA channels A (RGA 3) and B (RGA 1) respectively, and pitch and yaw outputs from the other two RGAs are routed through the righthand Aft IEA channels A (RGA 4) and B (RGA 2). Each pitch output and each yaw output from each RGA is routed through a separate twisted, shielded pair of wires with no internal IEA junction points and no outputs routed through a common connector at either end of the IEA.

D. Auxiliary Power Unit (APU) Fuel Control System

(1) Fuel Isolation Valve Circuit - To preclude loss of both TVC System due to loss of control signals to the Fuel Isolation Valves (FIVs) A and B per listed failure mode, redundant A and B channel solid state switches and wiring harnesses are provided. Normally closed FIVs are turned on via 3 amp 5 volt solid state switches in response to MDM commands. An open in the solid state switch or open or shorts in the wiring harness wires, internal connectors, external connectors, or junction modules would cause loss of FIV command resulting in APU shutdown. The Aft IEA design provides one common housing with a metal wall separating the redundant A and B channels. Design documentation for solid state switches is listed in Component/Design Description, Section 2 of this Appendix.

(2) Primary Speed Control Valve Circuit - To preclude loss of both TVC systems due to unscheduled control signals to the Primary Speed Control Valves (PCVs) A and B per listed failure mode, a redundant APU and APU control circuit is provided. A short of the APU Controller module card #1 valve control output or inadvertent operation of the APU BITE module card #1 would cause one PCV to close, resulting in APU shutdown. The Aft IEA design provides one common housing with a metal wall separating the redundant A and B channels.

(3) Secondary Speed Control Valve (Fuel Shut off valve-FSOV) Circuit -To preclude the loss of both TVC systems due to loss of control signals to the Fuel Shut Off Valves (FSOVs) A and B per listed failure mode, redundant APU Controller modules and power sources are provided. The APU Controller modules are turned on via 3 amp solid state switches (A2/B2 Start) in response to MDM commands. Loss of power to an APU Controller module or loss of and APU Controller module Card #2 (short or open) would cause one FSOV to close, resulting in APU shutdown and loss of redundancy for the TVC System. The Aft IEA design provides one common housing with a metal wall separating the redundant A and B channels so that no electrical failure can propagate from one channel to the other.

(4) For combination failures such as loss of APU speed control signal to the PCV and Unscheduled control signal to the FSOV on one APU (A or B). The PCV is a normally open valve in series with the FSOV, a normally closed valve, listed failure mode involves holding the PCV off and the FSOV on. Short circuits on the APU BITE module cards or the APU Controller module cards affecting both MPU inputs, open circuits in the wiring harness or APU Controller module cards affecting both MPU inputs, or a mixture of failures in the APU Controller module cards and/or the wiring carrying the valve commands could result in APU overspeed and turbine wheel fragmentation with loss of TVC and Fire in the Aft Skirt.

E. Hydraulic Pump Bypass Valve Circuit

To preclude unscheduled control signals to both TVC Systems Hydraulic Pump Bypass valves A and B, redundant A and B circuits with solid state switches are provided. Normally closed Hydraulic Pump Bypass valves are turned on via 3 amp 5 volt solid state switches in response to MDM commands. These valves are commanded open during APU start to allow the turbine drive to achieve full speed without a hydraulic pump load. Once the APUs reach full speed, the Bypass valves are closed, applying the pump output to the servoactuators. The Aft IEA design provides one common housing with a metal wall separating the redundant A and B channels so that no electrical failure can propagate from one channel to the other.

F. Servoactuator Command/Control Circuit

(1) Servovalve Command Circuit - To preclude the loss of TVC actuator servovalve commands per listed failure mode, separate, isolated wiring paths have been provided for each servovalve command. The Aft IEA design provides one common cast aluminum housing with a cast wall separating redundant A and B channels so that no electrical failure can propagate from one channel to the other. Within the Aft IEA, two command circuits are routed through each channel (A and B) as follows: A and C circuits are routed through channel A. B and D circuits are routed through channel B. Each TVC actuator command circuit is routed through a separate twisted shielded pair of wires with no internal IEA junction points. No two commands are routed through a common connector at either end of the IEA. Loss of Servovalve commands can result from shorts or opens in wiring path. The IEA is purged and pressurized with dry nitrogen, and wire routing is so controlled that no failure affecting one servovalve command channel can propagate to a second channel.

(2) Bypass Valve Command Circuit - To preclude the loss of TVC actuator servovalve bypass commands per listed failure mode, separate and isolated wiring paths have been provided for each of the four TVC

channels for all command and measurement lines. The Aft IEA design provides one common cast aluminum housing with a metal wall isolating the redundant A and B channels. Within the Aft IEA, two bypass circuits are routed through each IEA channel (A and B) as follows: A and C circuits are routed through IEA channel A. B and D circuits are routed through IEA channel B. Loss of TVC servovalve bypass commands can result from shorts or opens in the Wiring Paths. Each servovalve bypass command is routed through separate twisted wire pairs with no internal IEA junction points. No two TVC channels are routed through a common connector at either end of the IEA. The IEA is purged and pressurized with dry nitrogen, and wire routing is so controlled that no failure affecting one wire path can propagate to a wire path command.

(3) Delta Pressure Measurement Circuit - To preclude the loss of TVC actuator delta pressure measurements per listed failure mode, separate, isolated wiring paths have been provided for each of all four circuits for command and measurement lines. The Aft IEA design provides one common cast aluminum housing with a metal wall isolating the redundant A and B channels. Within the Aft IEA, two circuits are routed through each IEA channel (A and B) as follows: A and C circuits are routed through IEA channel A. B and D circuits are routed through IEA channel B. Loss of delta pressure measurements can result from shorts or opens in the wiring paths. Each delta pressure measurement line is routed through twisted shielded wire pairs with no internal IEA Junction points. Four excitation circuits are provided to the Aft IEA, and these go to junction points to provide four excitation channels to each actuator (Rock and Tilt). No two TVC channels are routed through a common connector at either end of the IEA. The IEA is purged and pressurized with dry nitrogen, and wire routing is so controlled that no failure affecting one wire path can propagate to a second wire path.

G. SRM Ignition Circuit

To preclude the loss of SRM ignition per listed failure mode, redundant A and B channel SRM ignition Fire 1 and Fire 2 wiring paths are routed through the Aft IEA with no breaks or junctions. The Aft IEA design provides one common housing with a metal wall isolating the redundant A and B channels. This failure mode could be caused by open or shorts in distributor wiring harnesses A and B. Failure of one or both paths cannot be detected prior to T-0 in launch countdown.

H. Separation System Circuits

(1) To preclude the loss of SRB separation per listed failure mode, redundant A and B separation channels are housed in the Aft Integrated Electronics Assembly (IEA). The Aft IEA design provides one common housing with a metal wall isolating the redundant A and B channels. The separation PICs accept signals from their respective A or B Separation Arm, Fire 1, and Fire 2 buses developed in the Aft IEA, and upon the proper sequence of commands, issue outputs to the A and B NSIs. The Separation Arm, Fire 1, and Fire 2 buses are developed by their respective Aft IEA A or B channel 0.5 amp combination solid state switches, which in turn are turned on by hardwired commands from the Orbiter. Power to the A or B Fire 2 Separation solid state switch is provided through a Miscellaneous IV Card diode from the A or B Fire 1, or Fire 2 test power solid state switch output. This design configuration assures that the Fire 2 inputs of the Separation PICs cannot be activated before Fire 1 inputs, thus preventing an unscheduled internal discharge of the PICs. Loss of separation function could be caused by open or short Separation solid state switches in the A and B channels, open or shorts in the A and B distributor harnesses, or open diodes on the Miscellaneous IV Cards. PIC failure causes with respect to these failure effects are addressed in other CIL sheets concerning loss of individual PICs. The failure of a PIC Arm function will be detected from flight data. The failure of a PIC Fire command circuit is not detectable in ascent.

(2) To preclude premature SRB separation, the system is designed to preclude the inadvertent operation of the SRB Separation ordnance. Series commands (Arm, Fire-1 and Fire- 2) with specific sequencing and timing are necessary to command SRB separation. The Arm command must occur at least 1 second before fire command. Fire-1 must precede or be coincident with Fire-2 at the PIC or the PIC will be discharged internally. The SRB Separation PICs are Armed approximately 1.7 seconds prior to separation to minimize the window of susceptibility for inadvertent SRB Separation ordnance firing, and allows the time required for sequencing through the SRB separation fire commands.

Parallel redundancy (dual redundant channels A and B) was implemented to assure SRB separation occurs when commanded. This failure mode, premature SRB separation, can be caused by failures in either of the redundant channels.

I. Booster Separation Motors (BSM) Circuits

(1) To preclude the loss of the Aft booster separation motor thrust per listed failure mode, parallel redundancy (dual redundant channels A and B) was implemented to assure SRB Aft BSM ignition occurs when commanded. The redundant A and B channel BSM ignition PICs are housed in the Aft Integrated Electronics Assembly (IEA). The Aft IEA design provides one common housing with a metal wall isolating the redundant A and B channels. These PICs accept signals from their respective A or B Separation Arm, Fire-1, and Fire-2 buses, and, upon the proper sequence of commands, issue outputs to the A and B aft BSM NSIs. The Separation Arm, Fire-1, and Fire-2 buses are energized by their respective Aft IEA A or B channel solid state switches turned on by the hardwired commands from the Orbiter. This failure mode could be caused by the loss of the A and B PICs or open or short in the A and B Distributor harnesses. Solid state switch failure causes with respect to this failure effect are addressed in the CIL concerning loss of the Separation PIC Arm, Fire-1, and Fire- 2 buses. The failure of a PIC Arm function will be detected from flight data during flight. The failure of a PIC Fire command circuit is not detectable as flight data is lost almost simultaneously with issuing of the separation commands. The failure mode, loss of SRB Aft BSM thrust, can occur only if both redundant A or B channels fail.

(2) To preclude unscheduled separation thrust, the system is designed to preclude the inadvertent operation of the SRB Aft BSMs. Series redundant commands (Arm, Fire-1 and Fire- 2) with specific sequencing and timing are necessary to energize SRB Aft BSM ignition. The Arm command must occur at least 1 second before fire command. Fire-1 must precede or be coincident with Fire-2 or the PIC will be discharged internally. The SRB BSM PICs are Armed approximately 1.7 seconds prior to separation to minimize the window of susceptibility for inadvertent SRB Aft BSM firing, and still allow time for the required sequencing to proceed for SRB separation fire commands. Due to the Parallel redundancy (Channels A & B), premature BSM firing can occur as a result of failures in either channel.

J. Strut Separation Bolt Circuits

The SRB Aft Separation A and B PICs (Upper, Middle and Lower) are housed in the Aft Integrated Electronics Assembly (IEA). The Aft IEA design provides one common, cast aluminum housing with a cast wall separating the redundant A and B channels such that no electrical failure can propagate from one channel to the other.

(1) To preclude the loss of the Aft upper, middle, or lower strut separation bolt PIC outputs per listed failure mode, redundant A and B channel upper, middle, and lower strut separation PICs are housed in the Aft Integrated Electronics Assembly (IEA). The Aft IEA design provides one common housing with a metal wall separating of the redundant A and B channels such that no electrical failure can propagate from one channel to the other. These PICs accept signals from their respective A or B Separation Arm, Fire-1, and Fire-2 buses, and, upon the proper sequence of commands, issue outputs to the A and B Aft upper,

middle, and lower strut separation bolt NSIs. The Separation Arm, Fire-1, and Fire-2 buses are energized by their respective Aft IEA A or B channel solid state switches which in turn are energized by the hardwired commands from the Orbiter. This failure mode could be caused by the loss of the A and B PICs or specific failures in the A and B Distributor harnesses. Solid state switch failure causes with respect to this failure effect are addressed in the CIL concerning loss of the Separation PIC Arm, Fire-1, and Fire-2 buses. The failure of a PIC Arm function will be detected from flight data during flight. The failure of a PIC Fire command is not detectable as flight data is lost almost simultaneously with issuing of the separation fire commands.

(2) To preclude premature separation, the system is designed to preclude the inadvertent firing of any SRB Aft Separation Bolt (Upper, Middle, or Lower). Series redundant commands (Arm, Fire-1 and Fire-2) with specific sequencing and timing are necessary to command SRB Separation. The Arm command must occur at least 1 second before fire command. Fire-1 must precede or be coincident with Fire-2 at the PIC or the PIC will be discharged internally. The SRB Separation PICs are Armed approximately 1.7 seconds prior to separation (the PIC requires 1 second to charge), to minimize the window of susceptibility of an inadvertent SRB Aft Separation Bolt PIC firing, but allow the required separation sequencing to proceed to SRB separation fire command.

Due to Parallel redundancy (dual redundant channels A and B) implemented to assure SRB Aft Separation occurs when commanded, premature SRB Aft Separation Bolt PIC output, can occur in either of the redundant channels.

K. Qualification

The Aft IEA, including specific hardware addressed for listed failure modes, was qualified to the environments specified in "Certification Test Requirements Specification" SE-019-107-2H and qualification certified on COQ #A-E&I-2120-2. The COQ lists the qualification test reports which comprise the total Aft IEA qualification effort. The qualification test environments which are most likely to induce this failure mode are:

-Vibration (Vehicle Dynamic, Lift-off, Re-entry)
-Shock (Ordnance, Water Entry)
-Thermal Cycling

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SECTION 2. COMPONENT DESIGN/ DESCRIPTION

A. Electronic Assembly

The electrical design of the EMC filters, transorb diodes, PBISs, APU Controller Modules, APU BITE Modules, and solid state switches uses the derating factors and high reliability parts in conformance with "EEE Parts Selection and Application Guidelines for Space Shuttle External Tank and Solid Rocket Booster," MSFC 85M03936 or "NASA Standard Electrical, Electronic, and Electromechanical Parts List," MIL-STD-975. Verification of the electrical design included "Worst Case" electrical, stress, and thermal analyses, considering component tolerances and stability through end of life, and environmental range of -10 degrees C to +100 degrees C. The mechanical packaging design is conservative, employing component mounting for stress free solder connections, high temperature printed wiring boards, and conformal coating in conformance with the following design requirements: (BI-1524 R3)

DOCUMENT NO	TITLE
MSFC-STD-136	Parts Mounting Design Requirements for Soldered Printed Wiring Board Assemblies
MSFC-STD-154A	Printed Wiring Boards (Copper Clad) Design, Documentation and Fabrication
MSFC-SPEC-278B	Terminals, Bifurcated and Turret, Swage Type: Terminals, Bifurcated and Turret, Standoff Insulated, Screw Type: Terminals, Solder Pot Swage Type
MSFC-SPEC-377C	Plastic Sheet, Laminated, Copper Clad (For Printed Wiring)
MSFC-SPEC-507	Low Solids (Thin) Conformal Coating Materials, PC Boards, Electronic and Electrical, Specification For (BI-1693 R1)
MSFC-PROC-274	Terminals, Installation of MSFC-PROC-508 Low Solids (Thin) Conformal Coating, Application of
MSFC-PROC-508	Low solids (thin) conformal coating, application of MSFC 50M60444 Plated Through Holes in Printed Wiring Boards, Specification For
NHB5300.4(3A/3A-1)	Requirements For Soldered Electrical Connections

B. EMC Filter

EMC filters are used at the AFT IEA power inputs to filter out electromagnetic "noise" and transients on the power lines. These filters also play a significant role in the suppression of lightning transients should they occur. All IEA power (except MDM power) passes through one of the two EMC filters (A or B). (Bus C provides no power to IEA functions and does not have an EMC Filter in the IEA.)

(1) An open circuit in both filters would remove all aft IEA power. This would cause two SRM chamber pressure measurements to go to null, and loss of power to two APUs, resulting in loss of vehicle control and improper SRB separation resulting in recontact with the orbiter/external tank.

(2) A short circuit in both filters would result in loss of power to all SRB operational electrical hardware, resulting in loss of Thrust Vector Control (TVC) during boost phase and loss of separation capability.

(3) An open circuit or short circuit in one filter combined with a failure in C bus would remove power from two SRM chamber pressure sensors and two rate gyros. This would cause SRM chamber pressure measurement to go to null, and could result in improper SRB separation causing recontact with the orbiter/external tank.

(4) An open circuit or short in the A or B filter combined with a failure in C bus would remove power from three SRB Rate Gyro Assemblies (RGAs) and could result in loss of rate detection in the pitch and yaw axes, causing loss of vehicle control.

EMC filters utilized in the IEA were designed specifically for the Shuttle SRB application. The applicable design documentation is listed below:

Design Document	Document Number
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311
EMC Filter Assembly Drawing	5100410/5100087
EMC Filter Schematic	5110410
EMC Filter Test Specification	5130410-GTS
EMC Filter Printed Wiring Board (PWB) Drawing	5107277

C. Transorb Lightning Suppressor Diode

The transorb diodes are used at the EMC filter outputs to "clamp" bus power and return lines with reference to chassis ground and prevent lightning transients from over-stressing IEA internal parts. A short circuit in both positive side transorb diodes (A and B) would result in the same failures as described for EMC filter shorts. The applicable design documentation is listed below:

Design Document	Document Number
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311
Transorb Assembly Drawing	5106985
Transorb Test Specification	5136704-GTS
Transorb PWB Drawing	5106983

D. Power Bus Isolation Supplies (PBIS)

PBISs are used to isolate and condition power for the IEA signal conditioner section. A short circuit in the power input portion of both PBISs would result in the same failures as described for EMC filter shorts. The applicable design documentation is listed below:

Design Document	Document Number
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311

Design Document	Document Number
PBIS Card 1 Assembly Drawing	5100384
PBIS Card 2 Assembly Drawing	5100385
PBIS Top Assembly Drawing	5106627
PBIS Schematic	5114827
PBIS Test Specification	5136521-GTS
PBIS Card 1 PWB Drawing	5105301
PBIS Card 2 PWB Drawing	5104426

E. Wiring Harness

The A and B sides of the Aft IEA distributor and signal conditioner wiring harnesses are physically and electrically isolated from each other by a metal wall. These wiring harnesses include wiring to distribute orbiter bus power (A, B, and C). Included in these harness assemblies are all connectors and junction modules. Bus C is routed through the A side of Aft IEA and is physically isolated from Bus A and B.

(1) A short circuit in lines on both A and B sides could result in loss of A, B, and C Bus Power to all SRB Functions..

(2) Loss of one of two wires, loss of one of two terminal blocks, or loss of specific pins in one connector would result in loss of redundant A or B buses to APU controller and other Aft IEA functions or Bus C to forward IEA..

(3) A short or open circuit in command and measurement lines will result in loss of specific input/output.

The design documentation is listed below:

Design Document	Document Number
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311
Distributor Wiring Harness A Assembly Dwg	5104122
Distributor Wiring Harness B Assembly Dwg	5104123
Signal Conditioner Wiring Harness A Assembly Drawing	5104124
Signal Conditioner Wiring Harness B Assembly Drawing	5104125
Distributor Wiring Harness A DITMCO Test	5114384-DTMC
Distributor Wiring Harness B DITMCO Test	5114393-DTMC
Signal Conditioner Wiring Harness A DIPMCO Test	5114324-DTMC
Signal Conditioner Wiring Harness B DITMCO Test	5114325-DTMC
Aft IEA Chassis Assembly Drawing	5104121
Aft IEA Chassis DITMCO Test	5114385-DTMC

Parts derating in wiring harness design is in accordance with "EEE Parts Selection and Application Guidelines for Space Shuttle External Tank and Solid Rocket Booster" (MSFC 85M03936) or NASA Standard Electrical, Electronic, and Electromechanical Parts List." Extensive tests and inspections occur during harness manufacture. Design requirements and specifications documents for the wiring harnesses are as follows:

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DOCUMENT NUMBER	
MIL-E-45782B	Specification for Electrical Wiring
40M39513/5	Electrical Wire, Insulated, High Temperature
40M39526/5	Electrical Cable, Shielded, Jacketed, General Specification For
40M38277	Connectors, Electrical, Circular, Miniature, High Density, Environmental Resisting
16A02980D	Connectors, Electrical, Circular, Miniature Underwater
MIL-B-5087B	Bonding, Electrical, and Lightning Protection, For Aerospace Systems
NHB5300.4(3A/3A-1)	Requirements for Soldered Electrical Connections
40M39589	Junctions and Junction Devices, Electrical Distribution and Bussing, Specification For
MSC/MSFC JD001	Crimping of Electrical Connections, Requirements For (BI-1836 R1)
1919269(PS)E	Flexible Epoxy Adhesive
10STD-0013	Retention Criteria Standard For Electrical Contacts

F. Solid State Switches

Solid state switches are used in the Aft IEA operational system for various functions requiring current gain, power isolation, and/or noise rejection. Switches are powered by orbiter bus voltage. Solid state switch modules are categorized by output current (3 amp or 0.5 amp) and by control voltage (5 volt, 28 volt, or combination). The Aft IEA uses 3 amp 5 volt, 0.5 amp 5 volt, 0.5 amp 28 volt, and 0.5 amp combination solid state switches connected to Orbiter buses.

(1) Short Circuit of Solid State Switch to ground/return will result in loss of Power Bus A or B to all SRB Functions.

(2) Open Solid State Switch will result in loss of output to serviced function.

(3) Internal short circuit of solid state switch across elements may result in unscheduled output to serviced functions.

The applicable design documentation is listed below:

Design Document	Document Number
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311
3 amp 5 volt Assembly Drawing	5100021
3 amp 5 volt Schematic	5110021
3 amp 5 volt Test Specification	5130021-GTS
3 amp 5 volt PWB Drawing	5120021
3 amp comb. Assembly Drawing	5100082

3 amp comb. Schematic	5110082
3 amp comb. Test Specification	5130082-GTS
3 amp comb. PWB Drawing	5120082
0.5 amp comb. Assembly Drawing	5100081
0.5 amp comb. Schematic	5110081
0.5 amp comb. Test Specification	5130081-GTS
0.5 amp comb. PWB Drawing	5120081

G. APU Bite Module

The APU Built In Test Equipment (BITE) module is an electronic module consisting of two similar BITE cards mounted on one common frame. Each BITE card on the module is designed to perform a resistance test on three magnetic coils (Fuel Control Valve coil, Fuel Shut Off Valve coil, Fuel Isolation Valve coil, pump bypass valve coil, and Magnetic Pickup Unit coils #1 and #2). Each BITE card on a BITE module is also designed to generate signals of specific frequencies simulating the operation of one MPU. The APU BITE module is designed so that only one of three APU fuel valves can be open at any given time during BITE tests. This is accomplished by sensing valve positions and generating high MPU simulator frequencies to cause the controller cards to sense high APU speed and close fuel valves. Each BITE card MPU signal simulator controls one APU fuel valve through the associated APU controller card. If an APU BITE card were to turn on during normal APU operation, its associated APU fuel valve would be closed in response to simulated MPU high frequency. (Two MDM commands, Power On and Regulator On, are required to turn on each APU BITE card.) If the MPU lines to an APU BITE card were to experience a logical short, the associated APU controller card would sense loss of APU speed and command its fuel valve open. The design documentation is listed below: (APU BITE)

<u>Design Document</u>	<u>Document Number</u>
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311
APU BITE Module Assembly Drawing	5105265
APU BITE Module Schematic	5114445
APU BITE Module Test Specification	5135265-GTS
APU BITE Card #1 PWB Drawing	5120206
APU BITE Card #2 PWB Drawing	5120207

H. APU Controller Module

The APU Controller module is an electronic module consisting of two similar control cards mounted on one common frame. Each control card is designed to monitor a Magnetic Pickup Unit (MPU) speed sensor which senses the shaft speed of the APU. Each control card has two outputs: a pulse signal at twice the shaft rotation rate which is used for telemetry, and a valve control output which operates one of the two series redundant APU fuel valves. The Fuel Control Valve (primary) is a normally open valve and cuts off APU fuel flow when energized. The Fuel Shut Off Valve (secondary) is a normally closed valve and cuts off APU fuel when deenergized. The control card for the primary valve (FCV) can control APU speed at 100 percent or 110 percent depending on system needs. The control card for the secondary valve (FSOV) will control the APU speed at 113 percent (if primary control has failed and the primary valve is in its normal open position). The design documentation is listed below: (APU Controller)

<u>Design Document</u>	<u>Document Number</u>
Design Requirements	5136100-CEI Part I
SRB Aft IEA Assembly	5080005-311
APU Controller Module Assembly Drawing	725451
APU Controller Module Schematic	725456

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APU Controller Module Test Specification	5137436-GTS
APU Controller Card #1 PWB Drawing	725452
APU Controller Card #2 PWB Drawing	725454

I. Miscellaneous IV Cards

The miscellaneous IV card provides resistors and diodes for various IEA functions. With respect to the Aft IEA Separation function, one diode on a miscellaneous IV card is utilized in A or B channel of the Aft IEA. Power to the A or B Fire-2 Separation solid state switch is provided through the diode from the A or B Fire-1 Solid state switch. This design configuration assures that the PIC Fire-2 input cannot be activated before the Fire-1 input, thus preventing an erroneous discharge of the PIC. An open diode can result in the loss of Separation A or B Fire-2 bus. The design documentation is listed below: (Miscellaneous IV Card Failure)

Design Document	Miscellaneous I
IEA CEI, Part I	5136100-CEI
SRB Aft IEA Assembly Drawing	5080005-311
Assembly Drawing	5100759
Schematic Drawing	5110759
Test Specification	5130759-GTS
Printed Wiring Board Drwg	5120759

J. Pyro Initiator Controller (PIC)

The Pyrotechnic Initiator Controller (PIC) contains a single channel, capacitor discharge energy, pyro-firing circuit; and built-in self test circuitry for a pyrotechnic initiator resistance test, and a pyrofiring load test. The electrical, electronic and electrical mechanical components are selected from or in accordance with the orbiter preferred parts list (OPPL) requirements. Component applications are evaluated to assure compliance with derating requirements. (PICs)(BI-1524 R3)(BI-1445)

The PIC design consists of two double-sided printed circuit boards attached to an aluminum frame and hard wired to an output connector. The design utilizes discrete solid-state components to satisfy circuit requirements.

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SECTION 3. TESTING

A. Acceptance Test- New Aft IEA

Acceptance Test - Aft IEA Acceptance Test are Conducted per Vendor Document 5135109-GTSP. All Production Units are Subjected to 100% Acceptance Testing which includes Visual examination, Isolation/Insulation Resistance and Dielectric Withstanding Voltage Test (Wiring Harness) and Specific Functional Testing Including:

(1) Application and redundancy verification of Power Buses A, B and through circuits.

(2) Verifying Series and Parallel Redundancy of the SRB Separation A and B System ARM, FIRE-1, FIRE-2 and FIRE- 2 Test Power Switches. (Includes Examination of operating Voltage, Timing, Currents, Output Wave Shapes, Loads/Circuit Resistance)

(3) Verifying Command and Measurement through circuits.

(4) Verifying Pyro Initiator Card (PIC) Charge and Discharge Time, Output energy and BITE Circuit operation.

(5) Verifying APU Fuel Control Valve Circuits.

(6) Verifying Hydraulic Pump Bypass Valve Control Circuit.

AFT IEA Acceptance Test includes Random Vibration (Operating) and Thermal (Functional test (+30 degrees F to + 135 degrees F). (All Failure Causes)

B. Recertification - Reused AFT IEA

(1) Repaired/ Refurbished IEA's - Aft IEA recertification will be accomplished to IEA Recertification Procedure III (vendor Document 5499296, which includes recertification to the same tests as the Aft IEA acceptance test (5135109-GTSP).

(2) Recycled/ Reused - Previously flown Aft IEAs will be recertified for reuse per 10SPC-0131 and 10REQ-0052. If anomalies are noted during recertification test, the IEA will be returned to the vendor for repair and acceptance testing.

(3) IEA's will be functionally tested prior to being placed in storage for reuse.

C. ESD Protection

ACO OMRSD 10REQ-0021, Para 4.11 requires that grounding wrist straps be worn at all times when electrical connector pins are being contacted with anything other than the mating connector and/or the component is being handled with covers removed. In addition, LRU connectors shall have metal caps or non-metallic ESD protective caps installed when not mated to cables, and prior to removing the LRU connector protective caps for cable mating. The shell of the mating connector shall be grounded. Interconnecting cables terminated on one end to an LRU are considered an extension of the LRU and are handled in accordance with the specified procedures.

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SECTION 4. VENDOR INSPECTION

The "Integrated Electronics Assembly, Inspection System Plan," 5499529, details the inspection plan for the Aft IEA. The inspections include raw materials, piece parts, subassembly, fabrication and final assembly. (All Failure Causes)

A. Electronic Assembly

Receiving inspection is performed to the individual component source control drawings. Transistors, optical couplers, diodes, and micro-circuits are 100 percent visually inspected. Capacitors, resistors, junction devices, card connectors and environmentally sealed connectors are sample inspected (1 percent Acceptable Quality Level [AQL]). External underwater connectors are 100 percent visually inspected per Acceptance/Rejection Criteria 5136849-GMS. Solder, flux, conformal coating, wire and copper clad board material are sample inspected upon receipt. USA SRBE QAR verifies material certification and receiving inspection/test records per SIP 1177. (All Failure Causes)

All the manufacturing inspection points of the Aft IEA are contained in AICL 5080005-311. Copies of the AICL remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177 for new build hardware and for refurbishment hardware. Inspections performed include the following: (All Failure Causes)

-Witness Load per vendor AICL
-Pre-covers Visual per vendor AICL
-Pre-MCO Visual per vendor AICL
-Room Temperature MCO per vendor 5135109-GTSP
-MCO Thermal per vendor 5136203-GMS

MCO testing (Room Temperature MCO and MCO Thermal) performs the same functional tests of the IEA as the acceptance test procedure (described below). Testing is performed at room temperature, +30 degrees F, and +135 degrees F and also includes 80 hours thermal cycling from +30 degrees F to +135 degrees F. (All Failure Causes)

All the Aft IEA acceptance inspection points are contained in AICL 5080005-311. Copies of the AICL remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177 for new build hardware and for refurbishment hardware. Inspections performed include the following: (All Failure Causes)

-ATP Thermal per vendor 5136202-GTP
-ATP Pressure Check per vendor AICL
-ATP Vibration per vendor 5136201-GTP
-Post Vibration Visual per vendor AICL
-Torque Inspection per vendor AICL
-Final ATP per vendor 5135109-GTSP
-Final Visual per vendor AICL

o Critical Processes/Inspections/Operations:

-Solder, Hand per 5136274-GMS
-Solder, Automatic per 5136900-GMS
-Component Staking per 5136239-GMS

-Conformal Coating per MSFC-PROC-508
-Crimping per 5136588-GMS
-Staking per 1919269(PS)
-Wire Retention Test per 5136737-GMS

B. EMC Filter

The in process inspections of the EMC filter are contained in Assembly Inspection Check List (AICL) 5100410. Copies of the AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (EMC Filters)

Kit Layout per vendor AICL
Solder Visual per vendor AICL
Pre-test per vendor 5130410-GTS
Post-test Visual per vendor AICL
Staking Visual per vendor AICL
Conformal Coating Visual per vendor AICL
Module Final Test per vendor 5130410-GTS
Module Final Visual per vendor AICL

Module final test per 5130410-GTS subjects the EMC filter to more stringent performance tests over a wider range of temperature (+14 degrees F to +212 degrees F) than is required of the Aft IEA (+30 degrees F to +135 degrees F). (EMC Filters)

C. Transorb Lightning Suppressor Diode

The in process inspections of the Transorb Diodes are contained in Assembly Inspection Check List 5106985. Copies of the AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (Transorb Diodes)

Kit Layout per vendor AICL
Solder Visual per vendor AICL
Pre-test per vendor 5136704-GTS
Post-test Visual per vendor AICL
Staking Visual per vendor AICL
Conformal Coating Visual per vendor AICL
Module Final Test per vendor 5136704-GTS
Module Final Visual per vendor AICL

Module final test per 5136704-GTS subjects the Transorb Diodes to more stringent performance tests over a wider range of temperature (+14 degrees F to +212 degrees F) than is required of the Aft IEA (+30 degrees F to +135 degrees F). (Transorb Diodes)

D. Power Bus Isolation Supplies

The in process inspections of the PBISs are contained in Assembly Inspection Check List 5106627. Copies of the AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (Power bus isolation Supplies)

Kit Layout per vendor AICL
Solder Visual per vendor AICL

Pre-test per vendor 5136521-GTS
Post-test Visual per vendor AICL
Staking Visual per vendor AICL
Conformal Coating Visual per vendor AICL
Module Final Test per vendor 5136521-GTS
Module Final Visual per vendor AICL

Module final test per 5136521-GTS subjects the PBIS module to more stringent performance tests over a wider range of temperature (+14 degrees F to +212 degrees F) than is required of the Aft IEA (+30 degrees F to +135 degrees F). (Power Bus Isolation Supplies)

E. Wiring Harness

The in process inspections of the IEA Distributor and Signal Conditioner Wiring Harnesses are contained in Assembly Inspection Check Lists as follows:

Distributor Wiring Harness A - 5104122
Distributor Wiring Harness B - 5104123
Signal Conditioner Wiring Harness A - 5104124
Signal Conditioner Wiring Harness B - 5104125

Copies of the AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (Wiring Harnesses)

Kit Layout per vendor AICL
Solder and Crimp Visual per vendor AICL
Insulation and Continuity Test (Distributor A) per vendor 5114384-DTMC
Insulation and Continuity Test (Distributor B) per vendor 5114383-DTMC
Insulation and Continuity Test (Signal Conditioner A) per vendor 5114324- DTMC
Insulation and Continuity Test (Signal Conditioner B) per vendor 5114325- DTMC
Wire Retention Test per vendor 5136737-GMS
Final Visual per vendor AICL

The in process inspection of the Aft IEA chassis assembly is contained in AICL 5104121. Copies of the AICL remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (Wiring Harnesses)

-Chassis Harness Installation and Staking per vendor AICL
-In Process and Solder Visual per vendor AICL
-Connector Installation and Torquing per vendor AICL
-Vibration Shake Test per vendor 5136201-GTP
-Insulation & Continuity Test per vendor 5114385-DTMC
-In Process Visual per vendor AICL
-Final Visual per vendor AICL

F. Solid State Switches

The in process inspections of the Solid State Switches are contained in Assembly Inspection Check Lists as follows:

3 amp 5 volt - 5100021
3 amp comb. - 5100082
0.5 amp comb. - 5100081

Copies of the AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (Solid State Switches)

Kit Layout per vendor AICL
Solder Visual per vendor AICL
3 amp 5 volt pre-test per vendor 5130021-GTS
3 amp comb. pre-test per vendor 5130082-GTS
0.5 amp comb. pre-test per vendor 5130081-GTS
Post-test Visual per vendor AICL
Staking Visual per vendor AICL
Conformal Coating Visual per vendor AICL
3 amp 5 volt module final test per vendor 5130021-GTS
3 amp comb. module final test per vendor 5130082-GTS
0.5 amp comb. module final test per vendor 5130081-GTS
Module Final Visual per vendor AICL

Module final test per 5130021-GTS, 5130082-GTS and 5130081- GTS subjects the Solid State Switch modules to more stringent performance tests over a wider range of temperature (+14 degrees F to +212 degrees F) than is required of the Aft IEA (+30 degrees F to +135 degrees F). (Solid State Switches

G. APU Bite Module

The in process inspections of the APU BITE Module are contained in Assembly Inspection Check List (AICL) 5105265. Copies of the AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177. Inspections performed include the following: (APU BITE)

Kit Layout per vendor AICL
Solder Visual per vendor AICL
APU BITE pre-test per vendor 5135265-GTS
Post-test Visual per vendor AICL
Staking Visual per vendor AICL
Conformal Coating Visual per vendor AICL
APU BITE module final test per vendor 5135265-GTS
Module Final Visual per vendor AICL

Module final test per 5135265-GTS subjects the APU BITE Module to more stringent performance tests over a wider range of temperature (+14 degrees F to +212 degrees F) than is required of the Aft IEA (+30 degrees F to +135 degrees F). (APU BITE)

H. APU Controller Module

Upon receipt, vendor QC performs a visual inspection of each APU Controller Module per 5104118 and a room temperature functional test per 5137436-GTS. USA SRBE QAR inspections are performed to SIP 1177. (APU Controller)

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I. Miscellaneous IV Card

The in process inspection points of the Miscellaneous IV card are contained in AICL, 5100759. (Miscellaneous IV Card Failures)

Copies of the respective AICLs remain with the hardware as it is processed through manufacturing and are retained. They define the inspection points performed by vendor. USA SRBE QAR inspections are performed to SIP 1177.
Inspections performed include:

-Kit Layout per vendor AICL
-Solder Visual per vendor AICL
-Pre-test per vendor 5130759-GTS
-Post-test Visual per vendor AICL
-Staking Visual per vendor AICL
- Conformal Coating Visual per vendor AICL
-Module Final Test per vendor 5130759-GTS
-Module Final Visual per vendor AICL

Module Final test per 5130759-GTS, subjects the Miscellaneous IV card to more stringent performance tests over a wider range of temperature (+14 degrees F to +212 degrees F) than is required of the Aft IEA.

J. Pyro Initiator Controller (PIC)

PIC Receiving inspections: Upon receipt, vendor QC performs a visual inspection of each PIC per 5104115 and a room temperature functional test per 5136115-GTS. USA SRBE QAR inspections are performed to SIP 1177.

Certification records and test reports are maintained certifying materials and physical properties. Receiving inspection performs visual and dimensional examinations of incoming parts. Electronic components are functionally tested prior to issue.

Fabrication is accomplished in a dedicated area which is environmentally controlled and has limited access. Contamination control procedures are verified by inspection.

Quality control verifies proper maintenance of the work area controls. Assembly/installation operations verified by inspection. Printed circuit boards are inspected under magnification after each soldering process for conformance to requirements. Parts identification verified by inspection. Electrostatic discharge protection is maintained. Measurement standards and processing equipment verified by inspection. Electrical terminations verified by inspection.

Printed circuit boards/soldering and inspected under magnification.

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SECTION 5. LRU (IEA) FIELD INSPECTIONS

A. ACO (USA SRBE) Inspections

(1) Aft IEA Receiving Inspection, Acceptance Data Package Review and External Connector Inspection is performed per ACO OMRSD 10REQ-0021 Para. 2.2.1.1.7.1 and 2.2.1.1.7.2 (All Failure Causes)

(2) USA SRBE Quality Assurance verifies the following Assembly Check Out (ACO) Testing:

(a) Aft IEA Bus A and B Power-on and Isolation. OMRSD 10REQ-0021 para. 2.2.2, 2.2.1.3, 2.2.2.1., and 2.2.2.1.1.

(b) Chamber Pressure Measurement Through Circuit Verification. OMRSD 10REQ-0021, Para. 2.2.2.7.5

(c) Rate Gyro Assembly Through Circuit Verification. OMRSD 10REQ-0021, para. 2.2.2.7.6

(d) HPU BITE Interlock test and Hot Fire Test Operationss verifies the APU Fuel Isolation Valve Control Circuit and Function. OMRSD 10REQ-0021, para. 2.3.4.3 & 2.3.16.2

(e) HPU BITE Interlock test and Hot Fire Test Operations verifies the APU Speed Control Valve Circuit and Function. OMRSD 10REQ-0021, para 2.3.4.3 & 2.3.16.2

(f) HPU BITE Interlock test and Hot Fire Test Operations verifies the APU Shutoff Valve Circuit and Function. OMRSD 10REQ-0021, para. 2.3.4.3 & 2.3.16.2

(g) HPU BITE Interlock test and Hot Fire Test Operations verifies the Hydraulic Pump Bypass Valve Circuit and Function. OMRSD 10REQ-0021, para 2.3.4.3 and 2.3.16.2

(h) TVC Servoactuator Command/Measurement Circuit and Functions. OMRSD 10REQ-0021. Para 2.3.14.

(i) SRM Ignition Through Circuit Verification. OMRSD 10REQ-0021, para 2.2.2.7.4

(j) IEA PIC BITE, Energy, and functional tests verify the Separation System Solid State Switches and Circuits. OMRSD 10REQ-0021, para 2.2.2.3. and 2.2.2.4

(k) SRB Booster Separation Motor Ignition A and B PIC Circuit Verification. OMRSD 10REQ-0021, para 2.2.2.4.3 and 2.2.2.4.4.

(l) IEA PIC BITE, Energy, and functional tests verify the AFT Separation Bolt PIC Circuit Verification. OMRSD 10REQ-0021, para. 2.2.2.3. & 2.2.2.4

B. KSC (SPC) Inspections

(1) SPC Quality Assurance Verifies the following Vehicle Testing and Data: (All Failure Causes)

(a) Orbiter to SRB Power Transfer verifies the Aft IEA Power Bus A and B Redundancy. OMRSD File II, Vol. I S00000.470 and S00FE0.230.

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(b) SRM Chamber Pressure Measurement System Verification. OMRSD File II, Vol. I S00000.450

(c) Rate Gyro Assembly Positive/Negative Torque Tests. OMRSD File II, Vol. I S00000.643 & S00FF0.230.

(d) APU Fuel Pump Bearing Soak Verifies Fuel Isolation Valve Control Circuit and Function. OMRSD File V, Vol. B42AP0.080.

(e) APU Frequency BITE Test Verifies the Speed Control Valve Circuit. OMRSD File V, Vol. I B42AP0.060.

(f) APU Frequency BITE Test Verifies the Shutoff Valve Circuit. OMRSD File V, Vol. I B42AP0.060

(g) APU Resistance BITE Test Verifies the Hydraulic Pump Bypass valve Circuit. OMRSD File V, Vol. I B42AP0.060

(h) TVC Servoactuator Gymbal Positioning Circuit Verification. OMRSD File II, Vol. I S00000.650 & S00FS0.030.

(i) SRM Ignition PIC Resistance and Arm & Fire Circuit Verification. File II Vol. I S00000.525, S00FA0.015, S00000.510

(j) Separation System PIC Resistance and Arm & Fire Circuit Verification. OMRSD File V, Vol. I B75PI0.011, File II, Vol. I S00000.525 and S00FA0.015.

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