CRITICAL ITEMS LIST

PROJECT: SRMS (-5 MCIU INSTALLED) SYSTEM: ELECTRICAL SUBSYSTEM
ASS'Y NOMENCLATURE: MCIU ASS'Y P/N: 51155F160-5 SHEET: 1

FMEA REF.	FMEA REV.	NAME, QTY, & DRAWING REF. DESIGNATION	FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	HDWR / FUNC. 2/1R CRITICALITY — RATIONALE FOR ACCEPTANCE SCREENS: A-PASS, B-PASS, C-PASS
2105	0	FAILURE DETECTOR QTY. 1. SCHEMATIC 812797	MODE: AUTOBRAKES DRIVE CIRCUIT FAILS TO "BRAKES OFF" FOR ONE OR MORE SOURCES. CAUSE(S): 1) SECOND BRAKE DRIVE FET OR CIRCUIT FAILS SHORTED 2) GPC OR MCIU SOFTWARE AUTOBRAKES LINE FAILS TO "BRAKE OFF". 3) SOFTWARE MCIU FAILURE WARNING AUTOBRAKES LATCH OUTPUT FAILS TO "BRAKE OFF". 4) H/W MCIU WATCHDOG TIMER/ HARDWIRED PROCESSOR FAILURE AUTOBRAKES LATCH OUTPUT FAILS TO "BRAKE OFF" 5) H/W MCIU WATCHDOG TIMER CIRCUIT FAILS LOW.	ASSOCIATED BITE VERIFICATION TEST WILL FAIL. FOR ALL CAUSES: ALL OPERATIONAL MODES ARE STILL AVAILABLE. CAUSE 1: BRAKES PULSE TEST WILL DETECT WHEN BRAKES ARE OFF. LOSS OF AUTOBRAKES FOR ALL SOURCES. CAUSE 2: BRAKES PULSE TEST WILL DETECT WHEN BRAKES ARE OFF. LOSS OF GPC INITIATED AUTOBRAKES. CAUSE 3: MCIU F.W. BITE VERIFICATION TEST WILL DETECT. LOSS OF AUTOBRAKES FOR SOFTWARE INITIATED MCIU FAILURE WARNING. CAUSE 4&5: MCIU H/W W.D. TIMER BITE VERIFICATION TEST WILL DETECT WHEN BRAKES ARE ON. LOSS OF AUTOBRAKES FOR H/W WATCHDOG TIMER/HARDWIRE PROCESSOR FAILURE. CAUSE 6: MCIU H/W W.D TIMER BITE VERIFICATION TEST WILL	DESIGN FEATURES --- THE BRAKE DRIVER IS IMPLEMENTED USING FET POWER TRANSISTORS, CONNECTED IN A SERIES REDUNDANT CONFIGURATION. THE CIRCUIT EMPLOYS CONTINUOUS TESTING TO VERIFY THE INTEGRITY OF THE BRAKE DRIVE CIRCUIT. THE O&C BRAKE SWITCH CONTROLS THE OPERATION OF THE BRAKE DRIVER THROUGH AN OPTO-ISOLATOR WHICH ACTS AS A SOLID-STATE RELAY. OPTO-ISOLATORS (DIODE AND TRANSISTOR) MEET THE SAME QUALITY AND APPLICATION CRITERIA THAT HAVE BEEN APPLIED TO DISCRETE SEMICONDUCTORS. INDUCTORS ARE DESIGNED SPECIFICALLY FOR THE APPLICATION. THE DESIGN CRITERIA, INCLUDING CHOICE OF MATERIALS AND TEST REQUIREMENTS ARE IN ACCORDANCE WITH MIL-T-27. WORST CASE STRESS LEVELS DO NOT EXCEED THOSE ALLOWED BY SPAR-RMS-PA.003. ALL RESISTORS AND CAPACITORS USED IN THE DESIGN ARE SELECTED FROM ESTABLISHED RELIABILITY (ER) TYPES. LIFE EXPECTANCY IS INCREASED BY ENSURING THAT ALL ALLOWABLE STRESS LEVELS ARE DERATED IN ACCORDANCE WITH SPAR-RMS-PA.003. ALL CERAMIC AND ELECTROLYTIC CAPACITORS ARE ROUTINELY SUBJECTED TO RADIOGRAPHIC INSPECTION. DISCRETE SEMICONDUCTOR DEVICES SPECIFIED TO AT LEAST THE TX LEVEL OF MIL-S-19500. ALL DEVICES ARE SUBJECTED TO RE-SCREENING BY AN INDEPENDANT TEST HOUSE. SAMPLES OF ALL PROCURED LOTS/DATE CODES ARE SUBJECTED TO DESTRUCTIVE PHYSICAL ANALYSIS (DPA) TO VERIFY THE INTEGRITY OF THE MANUFACTURING PROCESSES. DEVICE STRESS LEVELS ARE, DERATED IN ACCORDANCE WITH SPAR-RMS-PA.003 AND VERIFIED BY DESIGN REVIEW. THE DESIGN UTILIZES PROVEN CIRCUIT TECHNIQUES AND IS IMPLEMENTED USING CMOS LOGIC DEVICES. CMOS DEVICES OPERATE AT LOW POWER AND HENCE DO NOT EXPERIENCE SIGNIFICANT OPERATING STRESSES. THE TECHNOLOGY IS MATURE, AND DEVICE RELIABILITY HISTORY IS WELL DOCUMENTED. ALL STRESSES ARE ADDITIONALLY REDUCED BY DERATING THE APPROPRIATE PARAMETERS IN ACCORDANCE WITH SPAR-RMS-PA.003. SPECIAL HANDLING PRECAUTIONS ARE USED AT ALL STAGES OF MANUFACTURE TO PRECLUDE DAMAGE/STRESS DUE TO ELECTROSTATIC DISCHARGE. THE DIODE AND TRANSISTOR, WHICH COMPRISE AN OPTO-ISOLATOR, ARE SUBJECTED TO THE SAME QUALITY AND APPLICATION CONTROLS AS APPLIED TO DISCRETE SEMICONDUCTORS. THE BRAKING LOGIC CIRCUIT IS MADE UP OF CMOS, AN INDUCTOR, AND RESISTORS AND DIODES.

PREPARED BY: MFWG SUPERCEDING DATE: NONE DATE: 11 JUL 91 CIL REV: 0

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ASS'Y NOMENCLATURE: MCIU ASS'Y P/N: 51155F160-5 SHEET: 2

FMEA REF.	FMEA REV.	NAME, QTY, & DRAWING REF. DESIGNATION	FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	HDWR / FUNC. 2/1R CRITICALITY — RATIONALE FOR ACCEPTANCE SCREENS: A-PASS, B-PASS, C-PASS
2105	0	MICRO-COMPUTER QTY. 1 CPU -SCHEMATIC 812806 RAM AND PARITY-SCHEMATIC 812804 EPROM-SCHEMATIC 813357	MICRO COMP --- 6) HARDWIRED PROCESSOR FAILURE CIRCUIT FAILS LOW.	DETECT WHEN BRAKES ARE ON. LOSS OF AUTOBRAKES FOR HARDWIRED PROCESSOR FAILURE. WORST CASE --- LOSS OF AUTOBRAKING. SYSTEM UNPROTECTED FROM RUNAWAY. ANNUNCIATED. REDUNDANT PATHS REMAINING --- 1) MANUAL BRAKES (FOR SAFING THE SYSTEM). 2) DIRECT DRIVE (FOR CONTINUING OPERATIONS).	ACCEPTANCE TESTS --- THE MCIU IS SUBJECTED TO THE FOLLOWING ACCEPTANCE ENVIRONMENTAL TESTING AS AN LRU. O VIBRATION: LEVEL AND DURATION - REFERENCE TABLE 3.2 O THERMAL: +40 DEGREES C TO -16 DEGREES C (2 CYCLES) QUALIFICATION TESTS --- THE MCIU IS SUBJECTED TO THE FOLLOWING LRU QUALIFICATION ENVIRONMENTS: O VIBRATION: LEVEL AND DURATION - REFERENCE TABLE 3.2 O SHOCK: BY SIMILARITY TO -3 MCIU O THERMAL: +51 DEGREES C TO -27 DEGREES C (10 CYCLES) O HUMIDITY: BY SIMILARITY TO -3 MCIU O EMC: MIL-STD-461 AS MODIFIED BY SL-E-0002 (TESTS CE01, CE03, CS01, CS02, CS06, RE02 (N/B), RS01, RS02 O LIFE: 630 OPERATING HOURS 1000 POWER ON/OFF CYCLES FLIGHT CHECKOUT --- PDRS OPS CHECKLIST (ALL VEHICLES) JSC 16987

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CRITICAL ITEMS LIST

PROJECT: SRMS (-5 MCIU INSTALLED) SYSTEM: ELECTRICAL SUBSYSTEM
ASS'Y NOMENCLATURE: MCIU ASS'Y P/N: 51155F160-5 SHEET: 3

FMEA REF.	FMEA REV.	NAME, QTY, & DRAWING REF. DESIGNATION	FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	HDWR / FUNC. 2/1R CRITICAL.TY — RATIONALE FOR ACCEPTANCE SCREENS: A-PASS, B-PASS, C-PASS
2105	0	FAILURE DETECTOR QTY. 1. SCHEMATIC 812797	MODE: AUTOBRAKES DRIVE CIRCUIT FAILS TO "BRAKES OFF" FOR ONE OR MORE SOURCES. CAUSE(S): 1) SECOND BRAKE DRIVE FET OR CIRCUIT FAILS SHORTED 2) GPC OR MCIU SOFTWARE AUTOBRAKES LINE FAILS TO "BRAKE OFF". 3) SOFTWARE MCIU FAILURE WARNING AUTOBRAKES LATCH OUTPUT FAILS TO "BRAKE OFF". 4) H/W MCIU WATCHDOG TIMER/ HARDWIRED PROCESSOR FAILURE AUTOBRAKES LATCH OUTPUT FAILS TO "BRAKE OFF" 5) H/W MCIU WATCHDOG TIMER CIRCUIT FAILS LOW.	ASSOCIATED BITE VERIFICATION TEST WILL FAIL. FOR ALL CAUSES: ALL OPERATIONAL MODES ARE STILL AVAILABLE. CAUSE 1: BRAKES PULSE TEST WILL DETECT WHEN BRAKES ARE OFF. LOSS OF AUTOBRAKES FOR ALL SOURCES. CAUSE 2: BRAKES PULSE TEST WILL DETECT WHEN BRAKES ARE OFF. LOSS OF GPC INITIATED AUTOBRAKES. CAUSE 3: MCIU F.W. BITE VERIFICATION TEST WILL DETECT. LOSS OF AUTOBRAKES FOR SOFTWARE INITIATED MCIU FAILURE WARNING. CAUSE 4&5: MCIU H/W W.D. TIMER BITE VERIFICATION TEST WILL DETECT WHEN BRAKES ARE ON. LOSS OF AUTOBRAKES FOR H/W WATCHDOG TIMER/HARDWIRE PROCESSOR FAILURE. CAUSE 6: MCIU H/W W.D TIMER BITE VERIFICATION TEST WILL	QA/INSPECTIONS --- DOCUMENTED QUALITY CONTROLS ARE EXERCISED THROUGHOUT DESIGN PROCUREMENT, PLANNING, RECEIVING, PROCESSING FABRICATION, ASSEMBLY, TESTING AND SHIPPING OF THE MCIU. GOVERNMENT SOURCE INSPECTION IS INVOKED AT VARIOUS LEVELS OF COMPONENT ASSEMBLY AND TEST OPERATIONS. MANDATORY INSPECTION POINTS ARE EMPLOYED AT VARIOUS LEVELS OF ASSEMBLY AND TEST. EEE PARTS INSPECTION IS PERFORMED AS REQUIRED BY SPAR-RMS-PA.003. EACH EEE PART IS QUALIFIED AT THE PART LEVEL TO THE REQUIREMENTS OF THE APPLICABLE SPECIFICATION. ALL EEE, PARTS ARE 100% SCREENED AND BURNED IN, AS A MINIMUM, AS REQUIRED BY SPAR-RMS-PA.003, BY THE SUPPLIER. ADDITIONALLY, EEE PARTS ARE 100% RE-SCREENED IN ACCORDANCE WITH REQUIREMENTS, BY AN INDEPENDENT SPAR APPROVED TESTING FACILITY. DPA IS PERFORMED AS REQUIRED BY PA.003 ON A RANDOMLY SELECTED 5% OF PARTS, MAXIMUM 5 PIECES, MINIMUM 3 PIECES FOR EACH LOT NUMBER/DATE CODE OF PARTS RECEIVED. WIRE IS PROCURED, INSPECTED, AND TESTED TO SPAR-RMS-PA.003. RECEIVING INSPECTION VERIFIES THAT ALL PARTS RECEIVED ARE AS IDENTIFIED IN THE PROCUREMENT DOCUMENTS, THAT NO PHYSICAL DAMAGE HAS OCCURRED TO PARTS DURING SHIPMENT, THAT THE RECEIVING DOCUMENTS PROVIDE ADEQUATE TRACEABILITY INFORMATION AND SCREENING DATA CLEARLY IDENTIFIES ACCEPTABLE PARTS. PARTS ARE INSPECTED THROUGHOUT MANUFACTURE AND ASSEMBLY AS APPROPRIATE TO THE MANUFACTURING STAGE COMPLETED. THESE INSPECTIONS INCLUDE, PRINTED CIRCUIT BOARD INSPECTION FOR TRACK SEPARATION, DAMAGE AND ADEQUACY OF PLATED THROUGH HOLES, COMPONENT MOUNTING INSPECTION FOR CORRECT SOLDERING, WIRE LOOPING, STRAPPING, ETC. OPERATORS AND INSPECTORS ARE TRAINED AND CERTIFIED TO NASA NHB 5300.4(3A-1) STANDARD. CONFORMAL COATING INSPECTION FOR ADEQUATE PROCESSING IS PERFORMED USING ULTRAVIOLET LIGHT TECHNIQUES. POST P.C. BD. INSTALLATION INSPECTION, CLEANLINESS AND WORKMANSHIP (SPAR/GOVERNMENT REP. MANDATORY INSPECTION POINT) P.C. BD. INSTALLATION INSPECTION, CHECK FOR CORRECT BOARD INSTALLATION, ALIGNMENT OF BOARDS, PROPER CONNECTOR CONTACT MATING, WIRE ROUTING, STRAPPING OF WIRES ETC., PRE-CLOSURE INSPECTION, WORKMANSHIP AND CLEANLINESS (SPAR/GOVERNMENT REP. - MANDATORY INSPECTION POINT) PRE-ACCEPTANCE TEST INSPECTION, WHICH INCLUDES AN AUDIT OF LOWER TIER INSPECTION COMPLETION, AS BUILT CONFIGURATION VERIFICATION TO AS DESIGN ETC., (MANDATORY INSPECTION POINT). A TEST READINESS REVIEW (TRR) WHICH INCLUDES VERIFICATION OF TEST PERSONNEL, TEST DOCUMENTS, TEST EQUIPMENT CALIBRATION/ VALIDATION STATUS AND HARDWARE CONFIGURATION IS CONVENED BY

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ASS'Y NOMENCLATURE: MCIU ASS'Y P/N: 51155F160-5 SHEET: 4

FMEA REF.	FMEA REV.	NAME, QTY, & DRAWING REF. DESIGNATION	FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	HDWR / FUNC. 2/1R CRITICALITY — RATIONALE FOR ACCEPTANCE SCREENS: A-PASS, B-PASS, C-PASS
2105	0	MICRO-COMPUTER QTY. 1 CPU -SCHEMATIC B12806 RAM AND PARITY-SCHEMATIC B12804 EPROM-SCHEMATIC B13357	MICRO COMP --- 6) HARDWIRED PROCESSOR FAILURE CIRCUIT FAILS LOW.	DETECT WHEN BRAKES ARE ON. LOSS OF AUTOBRAKES FOR HARDWIRED PROCESSOR FAILURE. WORST CASE --- LOSS OF AUTOBRAKING. SYSTEN UNPROTECTED FROM RUNAWAY. ANNUNCIATED. REDUNDANT PATHS REMAINING --- 1) MANUAL BRAKES (FOR SAFING THE SYSTEN). 2) DIRECT DRIVE (FOR CONTINUING OPERATIONS).	QUALITY ASSURANCE IN CONJUNCTION WITH ENGINEERING, RELIABILITY, CONFIGURATION CONTROL, SUPPLIER AS APPLICABLE, AND THE GOVENNMENT REPRESENTATIVE, PRIOR TO THE START OF ANY FORMAL TESTING (ACCEPTANCE OR QUALIFICATION). ACCEPTANCE TESTING (ATP) INCLUDES AMBIENT, VIBRATION, AND THERMAL TESTING (SPAR/GOVERNMENT REP. - MANDITORY INSPECTION POINT).

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CRITICAL ITEMS LIST

PROJECT: SRMS (-5 MCIU INSTALLED) SYSTEM: ELECTRICAL SUBSYSTEM
ASS'Y NOMENCLATURE: MCIU ASS'Y P/N: 51155F160-5 SHEET: 5

FMEA REF.	FMEA REV.	NAME, QTY, & DRAWING REF. DESIGNATION	FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	HDWR / FUNC. 2/1R CRITICALITY	RATIONALE FOR ACCEPTANCE SCREENS: A-PASS, B-PASS, C-PASS
2105	0	FAILURE DETECTOR QTY. 1. SCHEMATIC B12797	MODE: AUTOBRAKES DRIVE CIRCUIT FAILS TO "BRAKES OFF" FOR ONE OR MORE SOURCES. CAUSE(S): 1) SECOND BRAKE DRIVE FET OR CIRCUIT FAILS SHORTED 2) GPC OR MCIU SOFTWARE AUTOBRAKES LINE FAILS TO "BRAKE OFF". 3) SOFTWARE MCIU FAILURE WARNING AUTOBRAKES LATCH OUTPUT FAILS TO "BRAKE OFF". 4) H/W MCIU WATCHDOG TIMER/ HARDWIRED PROCESSOR FAILURE AUTOBRAKES LATCH OUTPUT FAILS TO "BRAKE OFF" 5) H/W MCIU WATCHDOG TIMER CIRCUIT FAILS LOW.	ASSOCIATED BITE VERIFICATION TEST WILL FAIL. FOR ALL CAUSES: ALL OPERATIONAL MODES ARE STILL AVAILABLE. CAUSE 1: BRAKES PULSE TEST WILL DETECT WHEN BRAKES ARE OFF. LOSS OF AUTOBRAKES FOR ALL SOURCES. CAUSE 2: BRAKES PULSE TEST WILL DETECT WHEN BRAKES ARE OFF. LOSS OF GPC INITIATED AUTOBRAKES. CAUSE 3: MCIU F.W. BITE VERIFICATION TEST WILL DETECT. LOSS OF AUTOBRAKES FOR SOFTWARE INITIATED MCIU FAILURE WARNING. CAUSE 4&5: MCIU H/W W.D. TIMER BITE VERIFICATION TEST WILL DETECT WHEN BRAKES ARE ON. LOSS OF AUTOBRAKES FOR H/W WATCHDOG TIMER/HARDWIRE PROCESSOR FAILURE. CAUSE 6: MCIU H/W W.D TIMER BITE VERIFICATION TEST WILL	FAILURE HISTORY --- THERE HAVE BEEN NO FAILURES ASSOCIATED WITH THIS FAILURE MODE ON THE SRMS PROGRAM.	

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PROJECT: SRMS (-5 MCIU INSTALLED) SYSTEM: ELECTRICAL SUBSYSTEM
ASS'Y NOMENCLATURE: MCIU ASS'Y P/N: 51155F160-5 SHEET: 6

FMEA REF.	FMEA REV.	NAME, QTY, & DRAWING REF. DESIGNATION	FAILURE MODE AND CAUSE	FAILURE EFFECT ON END ITEM	HDWR / FUNC. 2/1R CRITICALITY — RATIONALE FOR ACCEPTANCE SCREENS: A-PASS, B-PASS, C-PASS
2105	0	MICRO-COMPUTER QTY. 1 CPU -SCHEMATIC 812806 RAM AND PARITY-SCHEMATIC 812804 EPROM-SCHEMATIC 813357	MICRO COMP --- 6) HARDWIRED PROCESSOR FAILURE CIRCUIT FAILS LOW.	DETECT WHEN BRAKES ARE ON. LOSS OF AUTOBRAKES FOR HARDWIRED PROCESSOR FAILURE. WORST CASE --- LOSS OF AUTOBRAKING. SYSTEM UNPROTECTED FROM RUNAWAY. ANNUNCIATED. REDUNDANT PATHS REMAINING --- 1) MANUAL BRAKES (FOR SAFING THE SYSTEM). 2) DIRECT DRIVE (FOR CONTINUING OPERATIONS).	OPERATIONAL EFFECT --- NO EFFECT BUT LOSS OF AUTOBRAKES FOR A SUBSEQUENT FAILURE. CREW ACTION --- SELECT DIRECT DRIVE IF WITHIN 10 FEET OF STRUCTURE. SINGLE/DIRECT DRIVE SWITCH SHOULD BE PULSED TO MAINTAIN PROPER RATES. CREW TRAINING --- CREW IS TRAINED TO ALWAYS OBSERVE WHETHER THE ARM IS RESPONDING PROPERLY TO COMMANDS. IF IT ISN'T, APPLY BRAKES. MISSION CONSTRAINT --- IF A FAILURE OF THE AUTO BRAKE FUNCTION IS DETECTED, COMPUTER SUPPORTED MODES SHOULD NOT BE USED. SCREEN FAILURES --- N/A OMRSD OFFLINE --- WITH BRAKE COMMAND LINE ON AND OFF, VERIFY NO BITE BITS ARE SET. OMRSD ONLINE INSTALLATION --- NONE OMRSD ONLINE TURNAROUND --- WITH BRAKE SWITCH ON AND OFF, VERIFY NO BITE BITS ARE SET.

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