SPAR - BRAMPTON (SSS)
9445 AIRPORT RD

BRAMPTON ONTARIO L6S4J3

Critical Items List

SRMS

CIL Ref#: 2581

Revision: 0 **FMEA Rev:** 0

System: SRMS

Subsystem: ELECTRICAL SUB-SYSTEM

Assembly Desc: Servo Power Amplifier

Part Number(s): 51140F1177-3 51140F1177-5

Item:		
Function:	Central Processing Unit Assembly	Provides hardware and software necessary to implement servo control loops, control operation of the Analog I/F, Digital I/F and MDA boards and communicate with the MCIU. Provides PLL and frame sync BITE as well as a hardware watchdog timer to monitor health of microcomputer itself.
	Motor Drive Amplifier Assembly	Provides motor voltage based on demand from tachometer electronics. Commutates the motor drive voltage. Provides hardware current limiting, brake drive, direct drive functions and enables backup drive. Provides BITE circuits and BITE verification for MDA.
	Analog Interface Assembly	Provides Tachometer excitation, SCU signal filtering, Phase Locked Loop and tachometer counter circuits to provide measured motor speed data to inner and outer rate loops. Provides analog to digital conversion of MDA buck output voltage, EPC +5V and reference voltages for BITE.
	Digital Interface Assembly	Receives and loads command data to CPU. Generates position encoder clock and sync signals, processes position encoder data and external flags and assembles return data for transmission to MCIU.

Failure Mode: CPU Halts.

	H/W	Func.	Screen Failures
Criticality:	2	1R	

Mission Phase: Orbit

Cause(s):	Analog Interface Assembly	Loss of inner rate loop timer interrupt.
	Central Processing Unit Assembly	CPU board select failed inactive (high).
		CPU bus transceiver read control failure.
		CPU off-board I/O analog select failed active (low).
		CPU off-board I/O CPU board select failed active (low).
		CPU off-board I/O MDA board select failed inactive (high).
		EDAC MBE flag failed active.
		Erroneous address bus data.
		Erroneous memory access cycles.
		I/O bus contention during I/O reads.
		I/O write failed to write state (high).
		Loss of ALE signal from microprocessor.
		Loss of BHE signal from microprocessor.

	Multiple data bit errors from SRAM.
	One or more microcomputer BITE hardware check signals fail active.
	Single bit error on memory databus.
	Single bit failure on microcomputer address/data bus.
	Unable to clear BITE status register.
	Unable to load Watchdog Word.
	Watchdog BITE fails active.
Digital Interface Assembly	IOW failed active.
Motor Drive Amplifier Assembly	Erroneous data from commutation FPGA for COM_DIRECTION flag.
	Incorrect inversion of RD0 register flags.
	Loss of inner rate loop timer interrupt.
	Loss of MDA data to CPU.
	MDASEL failed inactive (high).

Failure effect on unit/end item:

Microcomputer BITE bits are set via hardware. MCIU autobrakes. If failure occurs prior to power-up or when arm power is cycled SPA may fail to complete initialization leaving command and returned data shift registers cleared. For some causes CPU will operate correctly when brakes are OFF but will halt when brakes are ON. Direct drive remains available.

Worst Case: Unexpected motion. Joint runaway. Autobrakes.

Redundant Paths: Autobrakes (to Safe the System).
Direct Drive.
Backup Drive.
End Effector Auto mode (If Available).
End Effector Manual mode.

Retention Rationale

Design:

The Intel 80186 microprocessor is used in this design. This device, designed for use in conjunction with its corresponding high reliability support devices (EPROM, SRAM) comprises a processor kernal proven in many high reliability applications.

The design utilizes proven circuit techniques and is implemented using CMOS logic devices. CMOS devices operate at low power and hence do not experience significant operating stresses. The technology is mature, and device reliability history is well documented. All stresses are additionally reduced by derating the appropriate parameters in accordance with SPAR-RMS-PA.003. Special handling precautions are used at all stages of manufacture to preclude damage/stress due to electrostatic discharge.

Resistors and capacitors used in the design are selected from established reliability (ER) types. Life expectancy is increased by ensuring that all allowable stress levels are derated in accordance with SPAR-RMS-PA.003. All ceramic and electrolytic capacitors are routinely subjected to radiographic inspection in accordance with the requirements of MSFC-STD-355.

Field Programmable Gate Arrays (FPGA's) and the Error Detection and Correction (EDAC) are semi-custom microcircuits in which the basic

The SPA board is fabricated using Surface Mount Technology (SMT). This is a PWB assembly technology in which the components are soldered to the solder pads on the surface of the PWB. The significant advantage of this technology is to enable the parts on the board to be more densely packed, to reduce to overall volume and weight of the assembly.

The assembly process is highly automated. The parts are mounted on the boards using a computer controlled "pick and place" machine. The subsequent soldering operation is performed using a belt furnace, in which the time and temperature thermal profile that the PWB assembly is exposed to is tightly controlled and optimized to ensure proper part soldering attachment. The assembly is manufactured under documented procedures and quality controls. These controls are exercised throughout the assembly, inspection and testing of the unit. This inspection includes workmanship, component mounting, soldering, and conformal coating to ensure that it is in accordance with the NHB 5300 standards.

The SMT line used for the SPA PWB assembly has undergone a full qualification program, and assemblies produced on this line are used in other space programs.

The circuit board design has been reviewed to ensure adequate conductor width and separation and to confirm appropriate dimensions of solder pads and of component hold provisions. Parts mounting methods are controlled in accordance with MSFC-STD-154A, MSFC-STD-136 and SASD 2573751. These documents require approved mounting methods, stress relief and component security.

Test:

QUALIFICATION TESTS - The SPA is subjected to the following qualification testing:
VIBRATION: Each axis of the QM is subjected to Flight Acceptance Vibration Test (FAVT), Qualification Acceptance Vibration Test (QAVT), and Qualification Vibration Tests (QVT) in accordance with the SPA Vibration Test Procedure (826586). The level and duration for FAVT is as per Figure 6 and Table 2 of 826586; the level and duration for QAVT is as per Figure 7 and Table 2 of 826586; the level and duration for QVT is as per Figure 8 and Table of 826586. At the end of the three successive random vibration test in each axis, both directions (+/-) of each of the axis is subjected to a shock pulse test as per Figure 9 of 826586.
THERMAL/VACUUM: QM TVAC Test is in accordance with Figure 5 of the SPA TVAC Test Procedure (826588), with full Functional/Parametric Test performed at levels of +60 degrees C and -36 degrees C, and non-operating at -54 degrees C. The Qualification vacuum levels during TVAC is 1X10**-6 torr or less. The total test duration is 7 1/2 cycles. The QM SPA is subjected to a minimum of 1000 hours of life testing and 1000 power On-Off cycles.
EMC: The QM is subjected to EMC Testing (tests CE01/CE03, CE07, CS01, CS02, CS06, RE02, RS02, and RS03) in accordance with the SPA EMC test Procedure (826477) based on MIL-STD-461A.

UNIT FLIGHT ACCEPTANCE TESTS - The FM SPA is subjected to the following acceptance testing:
VIBRATION: FM Acceptance Vibration Test (AVT) in accordance with the SPA Vibration Test Procedure (826586), with level and duration as per Figure 6 and Table 2 of 826586.
THERMAL/VACUUM: FM TVAC Test is in accordance with Figure 6 of the SPA TVAC Test Procedure (826588), with levels of +49 degrees C and -25 degrees C for a duration of 1 1/2 cycles. The vacuum levels during Acceptance TVAC Test is 1X10**-5 torr or less.

JOINT SRU TESTS - The SPA is tested as part of the joints (ambient and vibration tests only). The ambient ATP for the Shoulder Joint, Elbow Joint, and Wrist Joint are as per ATP.2001, ATP.2003, and ATP.2005 respectively. The vibration test for the Shoulder Joint, and Elbow or Wrist Joint are as per ATP.2002, ATP.2004 and ATP.2006 respectively. Through wire function, continuity and electircal isolation tests are performed per TP.283.

MECHANICAL ARM REASSEMBLY - The SPA's/Joints undergo a mechanical arm integration stage where electrical checks are performed per TP.2007.

MECHANICAL ARM TESTING - The outgoing split-arm is configured on the Strongback and the Manipulator Arm Checkout is performed per ATP.1932.

FLIGHT CHECKOUT: PDRS OPS Checkout (all vehicles) JSC 16987.

Inspection:

Units are manufactured under documented quality controls. These controls are exercised throughout design procurement, planning, receiving, processing, fabrication, assembly, testing and shipping of the units. Mandatory inspection points are employed at various stages of

Unit Pre-Acceptance Test inspection, which includes an audit of lower tier inspection completion, as built configuration verification to as design etc (mandatory inspection point). A unit Test Readiness Review (TRR) which includes verification of test personnel, test documen test equipment calibration/validation status and hardware configuration is convened by QA in conjunction with Engineering, Reliability, Configuration Control, Supplier as applicable, and the government representative, prior to the start of any formal testing (Acceptance or Qualification). Unit level Acceptance Testing (ATP) includes ambient performance, thermal and vibration testing (Spar/government rep. mandatory inspection point).

Integration of unit to Joint SRU - Inspections include grounding checks, connectors for bent or pushback contacts, visual, cleanliness, interconnect wiring and power up test to the appropriate Joint Inspection Test Procedure (ITP). Joint level Pre-Acceptance Test Inspection, includes an audit of lower tier inspection completion, as built configuration verification to as design etc. Joint level Acceptance Testing (ATP) includes ambient and vibration testing (Spar/government rep. mandatory inspection point).

Mechanical Arm Reassembly - the integration of mechanical arm subassemblies to form the assembled arm. Inspections are performed at each phase of integration which includes electrical checks, through wiring checks, wiring routing, interface connectors for bent or pushback contacts etc. Mechanical Arm Testing - Strongback and flat floor ambient performance test (Spar/government rep. mandatory inspection point).

OMRSD Offline: Power-up arm. Verify no ABE communication failures or BITE errors.

OMRSD Online Installation: None

OMRSD Online Turnaround: Power-up arm. Verify no ABE communication failures or BITE errors.

Screen Failure: A: Pass
B: Pass
C: Pass

Crew Training: The crew will be trained to always observe whether the arm is responding properly to commands. If it isn't, apply brakes.

Crew Action: Select Direct Drive. Use EE Manual Mode. Single/Direct Drive switch should be pulsed to maintain proper rates.

Operational Effect: Cannot use computer supported modes of operation. Autobrakes. Direct Drive and Backup available. EE auto mode is unavailable. Arm will not stop automatically if failure of the auto brakes system has previously occurred. Brakes can be applied manually.

Mission Constraints: Operate under vernier rates within approximately 10 ft of structure. The operator must be able to detect that the arm is responding prope commands via window and/or CCTV views during all arm operations. Auto trajectories must be designed to come no closer than approxi 5 ft from structure.

Approvals:

Functional Group	Name	Position	Telephone	Date Signed	Status
Engineer	Hiltz, Michael / SPAR-BRAMPTON	Systems Engineer	4634	06Mar98	Signed
Reliability	Molgaard, Lena / SPAR-BRAMPTON	Reliability Engineer	4590	06Mar98	Signed
Program Management Offic	Rice, Craig / SPAR-BRAMPTON	Technical Program Manager	4892	06Mar98	Signed
Subsystem Manager	Glenn, George / JSC-ER	RMS Subsystem Manager	(281) 483-1516	30Mar98	Signed
Technical Manager	Allison, Ron / JSC-MV6	RMS Project Engineer JSC	(713) 483-4072	09Apr98	Signed

SAFETY + MISSION ASSURANCE CONN, DAVID / JSC-NC6 RMS SIMA ENGINEER (281) 483-3499 30 APR 98 David G. Conn